REMARKS

Claims 2, 3, 5, 6, 7 and 9 are pending. Claims 1, 4 and 8 have been canceled without prejudice or disclaimer. Claims 2, 5 and 7 have been amended. No new matter is presented.

Claim 2 has been amended to recite that the channel-forming semiconductor regions of the P-type MOS transistors are formed of a same deep N-type well so that these channel-forming semiconductor regions are electrically connected to each other. The channel-forming semiconductor regions of the N-type MOS transistors are formed of shallow P-type wells formed in the deep N-type well. Claim 2 also recites that the trenches are individually provided between the channel-forming semiconductor regions of the P-type and N-type MOS transistors, the trenches being deeper than the shallow P-type wells, but shallower than the deep N-type well. Support for these features can be found in Fig. 4 and at page 23, lines 6-24 of the specification.

The device of claim 2 provides that the area of the SRAM cell can be decreased as compared to the device disclosed in Hu (see Figs. 7 and 8 of Hu). Further, the number of processing steps for fabricating the cell can be decreased according to that which is claimed in claim 2. This reduces overall costs.

Claims 3, 5 and 7 depend from claim 2 and are allowable at least due to their respective dependencies.

Claim 9 was rejected under 35 USC 103(a) as being unpatentable over the admitted prior art and Hu and further in view of Hodges. This rejection is respectfully traversed.

Claim 9 recites "second MOS transistors ***for performing direct signal transmission and reception to and from an external device***." The second MOS transistors are each formed of a second well deeper than a first well forming the channel-forming semiconductor regions of the claimed first MOS transistor. The claimed first MOS transistor performs internal processing.

Applicant respectfully submits that none of the prior art references, either alone or in combination, teach or suggest a second MOS transistor which perform direct signal transmission to and from an external device and a first MOS transistor which performs internal processing. The Examiner has failed to specifically point out where these features are taught or suggested in any of the cited prior art. Applicant respectfully requests that the Examiner properly point out where these features are shown in the cited prior art or withdrawn this rejection.

Further, the Examiner has asserted that the motivation for combining the prior art references in this rejection is based solely on the fact that Hodges teaches peripheral circuitry and that Hu applies to that circuitry as well. Although how closely the prior art is related is one factor to consider, merely relating to the same field of technology is not in of itself proper motivation under 35 USC 103(a) to combine the references. There must be some evidence of a motivation to combine the references within the prior art. The Examiner has failed to provide any evidence other than the fact that the technology is the same or similar. This is insufficient. Applicant requests that this rejection be withdrawn.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge

the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 204552016500.

Respectfully submitted,

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By: Deborah S. Gladstein

Deborah S. Gladstein
Registration No. 43,636

Morrison & Foerster LLP
1650 Tysons Blvd., Suite 300
McLean, Virginia 22102
Telephone: (703) 760-7753
Facsimile: (703) 760-7777

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Cancel claims 1, 4 and 8.

Amend claims 2, 5 and 7 as follows:

2. (Amended) A static random access memory [as claimed in claim 1], wherein memory cells of the static random access memory each includes:

[an] N-type MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other; and

[a] P-type MOS transistors each having a channel-forming semiconductor region electrically connected with a power source,

wherein the channel-forming semiconductor regions of the P-type MOS transistors are formed of a same deep N-type well so that these channel-forming semiconductor regions are electrically connected to each other, and the channel-forming semiconductor regions of the N-type MOS transistors are formed of shallow P-type wells formed in the deep N-type well,

wherein trenches are individually provided between the channel-forming semiconductor regions of the P-type and N-type MOS transistors, said trenches being deeper than the shallow P-type wells, but shallower than the deep N-type well.

5. (Amended) A static random access memory as claimed in claim [1] 2, comprising write circuit means that include:

MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.

7. (Amended) A static random access memory as claimed in claim [1] 2, comprising read circuit means that include MOS transistors each having a channel-forming semiconductor region and a gate electrically connected with each other.